

# 深圳市英瑞达光电有限公司

---

## Specification for 2.13 inch EPD

**Model NO. : YRD213BBS800F41**

### Confirmation:

| Prepared by | Checked by | Approved by |
|-------------|------------|-------------|
|             |            |             |

### Customer approval:

| Customer | Approved by | Date |
|----------|-------------|------|
|          |             |      |

# 深圳市英瑞达光电有限公司

---

## Revision History

| Version | Content     | Date      | Producer |
|---------|-------------|-----------|----------|
| 2.0     | New release | 2024/11/4 |          |
|         |             |           |          |
|         |             |           |          |
|         |             |           |          |
|         |             |           |          |
|         |             |           |          |
|         |             |           |          |

# 深圳市英瑞达光电有限公司

---

## CONTENTS

|                                                                   |    |
|-------------------------------------------------------------------|----|
| 1. Over View .....                                                | 4  |
| 2. Features .....                                                 | 4  |
| 3. Mechanical and Optical Specification .....                     | 5  |
| 4. Mechanical Drawing of EPD Module .....                         | 6  |
| 5. Input/output Pin Assignment .....                              | 7  |
| 6. Electrical Characteristics .....                               | 8  |
| 6.1 Absolute Maximum Rating .....                                 | 8  |
| 6.2 Panel DC Characteristics .....                                | 9  |
| 6.3 Panel DC Characteristics(Driver IC Internal Regulators) ..... | 10 |
| 6.4 Panel AC Characteristics .....                                | 11 |
| 6.4.1 MCU Interface Selection .....                               | 11 |
| 6.4.2 MCU Serial Interface (4-wire SPI) .....                     | 11 |
| 6.4.3 MCU Serial Interface (3-wire SPI) .....                     | 13 |
| 6.4.4 Interface Timing .....                                      | 14 |
| 7.Command Table .....                                             | 16 |
| 8. Block Diagram .....                                            | 25 |
| 9. Typical Application Circuit with SPI Interface .....           | 26 |
| 10. Typical Operating Sequence .....                              | 27 |
| 10.1 LUT from OTP Operation Flow .....                            | 27 |
| 10.2 LUT from OTP Operation Reference Program Code .....          | 28 |
| 11. Reliability Test .....                                        | 29 |
| 12. Quality Assurance .....                                       | 30 |
| 12.1 Environment .....                                            | 30 |
| 12.2 Illuminance .....                                            | 30 |
| 12.3 Inspect method .....                                         | 30 |
| 12.4 Display area .....                                           | 30 |
| 12.5 Ghosting test method .....                                   | 30 |
| 12.6 Inspection standard .....                                    | 31 |
| 12.6.1 Electric inspection standard .....                         | 31 |
| 12.6.2 Appearance inspection standard .....                       | 32 |
| 13.Packaging .....                                                | 34 |
| 14. Handling, Safety, and Environment Requirements .....          | 35 |

---

## 1. Over View

YRD0213BBS800F41 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white and black full display capabilities. The 2.13 inch active area contains 250×122 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

## 2. Features

- ◆ 250×122 pixels display
- ◆ High contrast High reflectance
- ◆ Ultra wide viewing angle Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape portrait modes
- ◆ Hard-coat antiglare display surface
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform can stored in On-chip OTP or written by MCU
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I<sup>2</sup>C signal master interface to read external temperature sensor
- ◆ Built-in temperature sensor

# 深圳市英瑞达光电有限公司

## 3.Mechanical and Optical Specification

| Parameter           | Specifications          | Unit  | Remark  |
|---------------------|-------------------------|-------|---------|
| Screen Size         | 2.13                    | Inch  |         |
| Display Resolution  | 122(H)×250(V)           | Pixel | DPI:130 |
| Active Area         | 23.70×48.55             | mm    |         |
| Pixel Pitch         | 0.1942×0.1942           | mm    |         |
| Pixel Configuration | Rectangle               |       |         |
| Outline Dimension   | 29.2(H)×59.2(V) ×1.0(D) | mm    |         |
| Weight              | 3.2±0.5                 | g     |         |

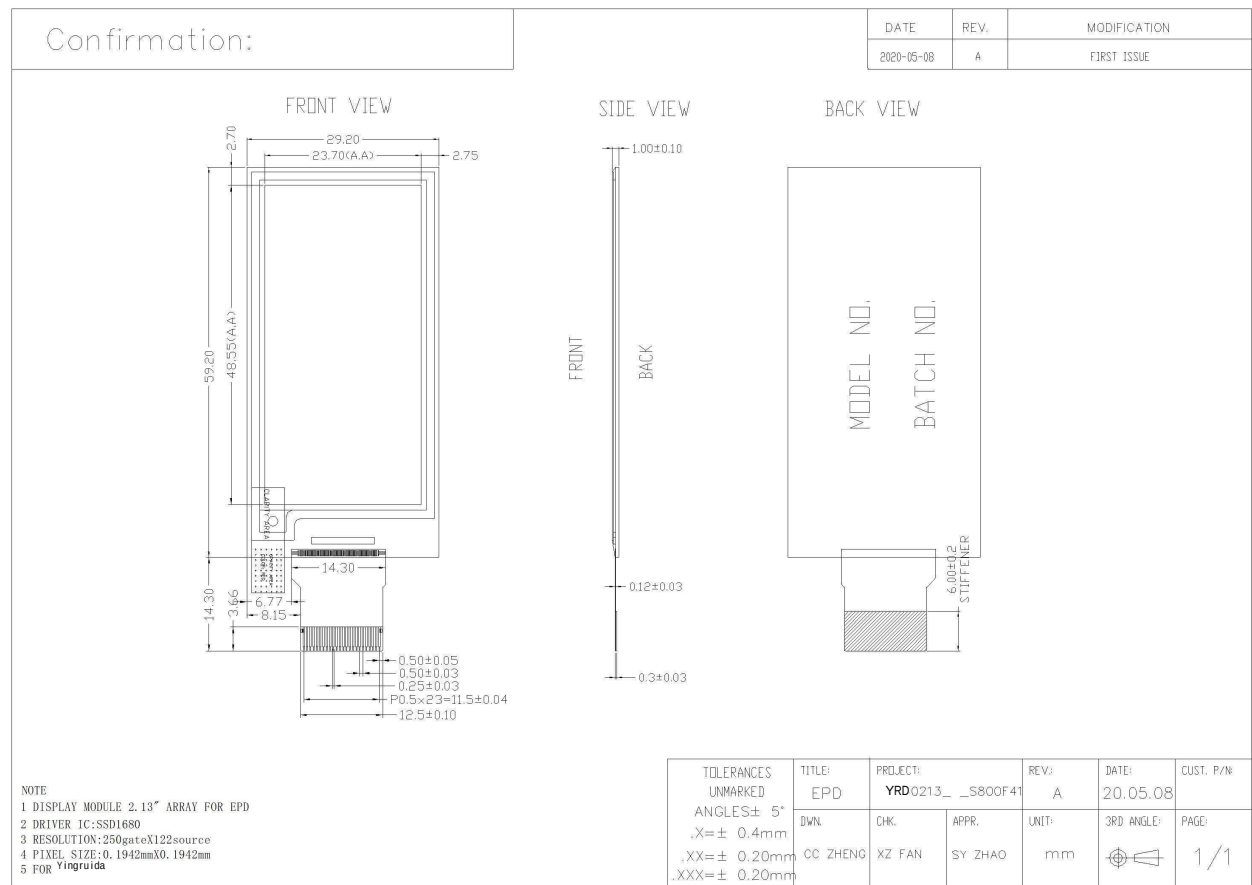
| Symbol | Parameter                 | Conditions                      | Min | Typ.   | Max | Units | Notes      |
|--------|---------------------------|---------------------------------|-----|--------|-----|-------|------------|
| KS     | Black State L* value      |                                 | -   | 24     | 30  |       | 3-1        |
| WS     | White State L* value      |                                 | 58  | 62     | -   |       | 3-1        |
|        | White Ghosting $\Delta L$ | Full Display Mode               | -   | 1      | -   |       | 3-1        |
|        |                           | Partil Display Mode             | -   | 1      | -   |       | 3-1        |
|        |                           | Full-Partil Display Mode        | -   | 1      | -   |       | 3-1        |
| R      | White Reflectivity        | White                           | 26  | 30     | -   | %     | 3-1        |
| CR     | Contrast Ratio            | Indoor                          | 5   | 7      | -   |       | 3-1<br>3-2 |
| GN     | 2Grey Level               | -                               | -   | -      | -   |       |            |
| Life   |                           | Temp:23±3℃<br>Humidity:55±10%RH |     | 5years |     |       | 3-3        |

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

3-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3-3. When the product is stored. The display screen should be kept white and face up.

4.Mechanical Drawing of EPD Module



# 深圳市英瑞达光电有限公司

## 5.Input/output Pin Assignment

| No. | Name  | I/O | Description                                                                                                        | Remark    |
|-----|-------|-----|--------------------------------------------------------------------------------------------------------------------|-----------|
| 1   | NC    |     | Do not connect with other NC pins                                                                                  | Keep Open |
| 2   | GDR   | O   | N-Channel MOSFET Gate Drive Control                                                                                |           |
| 3   | RESE  | I   | Current Sense Input for the Control Loop                                                                           |           |
| 4   | NC    | NC  | Do not connect with other NC pins                                                                                  | Keep Open |
| 5   | VSH2  | C   | Positive Source driving voltage 2                                                                                  |           |
| 6   | TSCL  | O   | I2C Interface to digital temperature sensor Clock pin                                                              | Note 5-6  |
| 7   | TSDA  | I/O | I2C Interface to digital temperature sensor Data pin                                                               | Note 5-6  |
| 8   | BS1   | I   | Bus Interface selection pin                                                                                        | Note 5-5  |
| 9   | BUSY  | O   | Busy state output pin                                                                                              | Note 5-4  |
| 10  | RES#  | I   | Reset signal input. Active Low.                                                                                    | Note 5-3  |
| 11  | D/C#  | I   | Data /Command control pin                                                                                          | Note 5-2  |
| 12  | CS#   | I   | Chip select input pin                                                                                              | Note 5-1  |
| 13  | SCL   | I   | Serial Clock pin (SPI)                                                                                             |           |
| 14  | SDA   | I/O | Serial Data pin (SPI)                                                                                              |           |
| 15  | VDDIO | P   | Power Supply for interface logic pins It should be connected with VCI                                              |           |
| 16  | VCI   | P   | Power Supply for the chip                                                                                          |           |
| 17  | VSS   | P   | Ground                                                                                                             |           |
| 18  | VDD   | C   | Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS |           |
| 19  | VPP   | P   | FOR TEST                                                                                                           | Keep Open |
| 20  | VSH1  | C   | Positive Source driving voltage                                                                                    |           |
| 21  | VGH   | C   | Power Supply pin for Positive Gate driving voltage and VSH1                                                        |           |
| 22  | VSL   | C   | Negative Source driving voltage                                                                                    |           |
| 23  | VGL   | C   | Power Supply pin for Negative Gate driving voltage VCOM and VSL                                                    |           |
| 24  | VCOM  | C   | VCOM driving voltage                                                                                               |           |

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

# 深圳市英瑞达光电有限公司

**Note 5-1:** This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

**Note 5-2:** This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

**Note 5-3:** This pin (RES#) is reset signal input. The Reset is active low.

**Note 5-4:** This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor

**Note 5-5:** Bus interface selection pin

| BS1 State | MCU Interface                                          |
|-----------|--------------------------------------------------------|
| L         | 4-lines serial peripheral interface(SPI) - 8 bits SPI  |
| H         | 3- lines serial peripheral interface(SPI) - 9 bits SPI |

**Note 5-6:** This pin connect to the VSS if there is no external temperature sensor.

External pull up resistor is required when connecting to I2C slave.

## 6. Electrical Characteristics

### 6.1 Absolute Maximum Rating

| Parameter                | Symbol    | Rating                         | Unit |
|--------------------------|-----------|--------------------------------|------|
| Logic supply voltage     | VCL,VDDIO | -0.5 to +6.0                   | V    |
| Logic Input voltage      | VIN       | -0.5 to V <sub>DDIO</sub> +0.5 | V    |
| Logic Output voltage     | VOUT      | -0.5 to V <sub>DDIO</sub> +0.5 | V    |
| Operating Temp range     | TOPR      | 0 to +50                       | °C.  |
| Storage Temp range       | TSTG      | -25 to+70                      | °C.  |
| Optimal Storage Temp     | TSTGo     | 23±2                           | °C.  |
| Optimal Storage Humidity | HSTGo     | 55±10                          | %RH  |

**Note:**

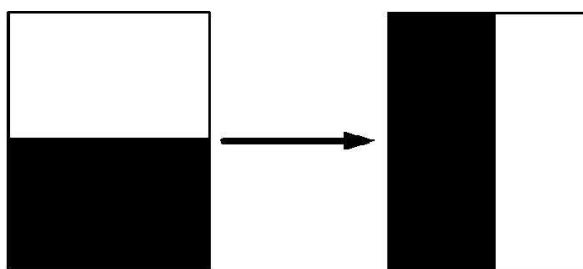
1. Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.
2. The display screen should be kept white and face up during storage. Please refer to the [Reliability Test] section.

## 6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR = 23°C.

| Parameter                      | Symbol            | Condition                                                     | Applicable pin    | Min.                     | Typ.   | Max.                     | Unit |
|--------------------------------|-------------------|---------------------------------------------------------------|-------------------|--------------------------|--------|--------------------------|------|
| Single ground                  | V <sub>SS</sub>   | -                                                             |                   | -                        | 0      | -                        | V    |
| Logic supply voltage           | V <sub>CI</sub>   | -                                                             | V <sub>CI</sub>   | 2.2                      | 3.0    | 3.7                      | V    |
| Power for interface logic pins | V <sub>DDIO</sub> |                                                               | V <sub>DDIO</sub> | 2.2                      | -      | 3.7                      | V    |
| Core logic voltage             | V <sub>DD</sub>   |                                                               | V <sub>DD</sub>   | 1.7                      | 1.8    | 1.9                      | V    |
| VCOM_DC output voltage         | V <sub>com</sub>  | -                                                             | VCOM              | -                        | -      | -                        | V    |
| High level input voltage       | V <sub>IH</sub>   | -                                                             | -                 | 0.8<br>V <sub>DDIO</sub> | -      | -                        | V    |
| Low level input voltage        | V <sub>IL</sub>   | -                                                             | -                 | -                        | -      | 0.2<br>V <sub>DDIO</sub> | V    |
| High level output voltage      | V <sub>OH</sub>   | IOH = -100uA                                                  | -                 | 0.9<br>V <sub>DDIO</sub> | -      | -                        | V    |
| Low level output voltage       | V <sub>OL</sub>   | IOL = 100uA                                                   | -                 | -                        | -      | 0.1<br>V <sub>DDIO</sub> | V    |
| Typical power                  | P <sub>TYP</sub>  | V <sub>CI</sub> = 3.0V                                        | -                 | -                        | 12     | -                        | mW   |
| Deep sleep mode                | P <sub>STPY</sub> | V <sub>CI</sub> = 3.0V                                        | -                 | -                        | 0.0009 | -                        | mW   |
| Typical operating current      | Iopr_VCI          | V <sub>CI</sub> = 3.0V                                        | -                 | -                        | 4      | -                        | mA   |
| Image update time              | -                 | 23 °C                                                         | -                 | -                        | 4      | -                        | sec  |
| Typical peak current           | Iopr_VCI          | 2.3~3.6v                                                      |                   |                          | 30     | -                        | mA   |
| Deep sleep mode current        | Idslp_VCI         | DC/DC off<br>No clock<br>No input load<br>Ram data not retain | -                 | -                        | 0.3    | 3                        | uA   |

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



- The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
- The listed electrical characteristics are only guaranteed under the controller & waveform provided by Yingruida.
- Electrical measurement: Tektronix oscilloscope - MDO3014,  
Tektronix current probe - TCP0030A.

# 深圳市英瑞达光电有限公司

## 6.3 Panel AC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23°C.

| Parameter                      | Symbol          | Condition                                                                                                                                                                                                                         | Applicable pin                   | Min.  | Typ. | Max.  | Unit |
|--------------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|-------|------|-------|------|
| VCOM output voltage            | VCOM            | VCI=3.0V<br>Enable Clock and Analog by Master Activation<br>Command<br>VGH=20V<br>VGL=-VGH<br>VSH1=15V<br>VSH2=5V<br>VSL=-15V<br>VCOM = -2V<br>No waveform transitions.<br>No loading.<br>No RAM read/write<br>No OTP read /write | VCOM                             | -2.2  | -2   | -1.8  | V    |
| Positive Source output voltage | V <sub>SH</sub> |                                                                                                                                                                                                                                   | S <sub>0</sub> ~S <sub>127</sub> | +14.8 | +15  | +15.2 | V    |
| Negative Source output voltage | V <sub>SL</sub> |                                                                                                                                                                                                                                   | S <sub>0</sub> ~S <sub>127</sub> | -15.2 | -15  | -14.8 | V    |
| Positive gate output voltage   | V <sub>gh</sub> |                                                                                                                                                                                                                                   | G <sub>0</sub> ~G <sub>295</sub> | +19.5 | +20  | +20.5 | V    |
| Negative gate output voltage   | V <sub>gl</sub> |                                                                                                                                                                                                                                   | G <sub>0</sub> ~G <sub>295</sub> | -20.5 | -20  | -19.5 | V    |

## 6.4 MCU Interface

### 6.4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

| Pin Name         | Data/Command Interface |     | Control Signal |      |      |
|------------------|------------------------|-----|----------------|------|------|
| Bus interface    | SDA                    | SCL | CS#            | D/C# | RES# |
| BS1=L 4-wire SPI | SDA                    | SCL | CS#            | D/C# | RES# |
| BS1=H 3-wire SPI | SDA                    | SCL | CS#            | L    | RES# |

Table 6-4-1: MCU interface assignment under different bus interface mode

### 6.4.2 MCU Serial Interface (4-wire SPI)

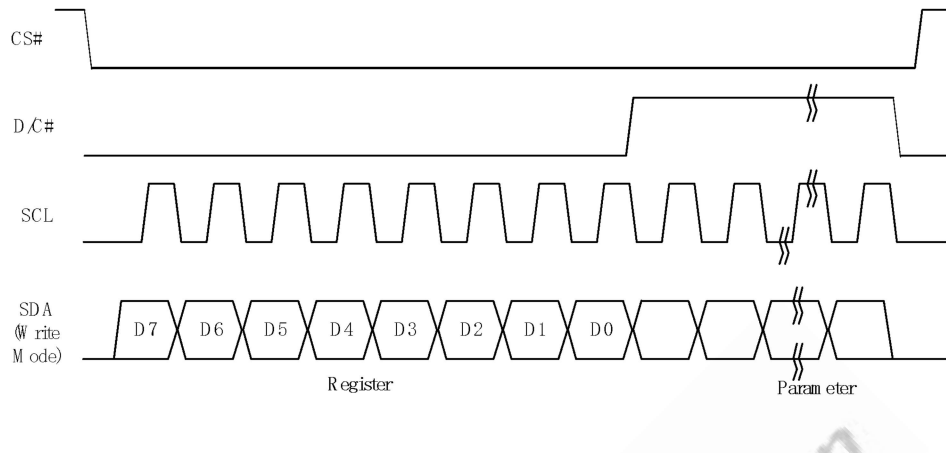
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

| Function      | CS# | D/C# | SCL |
|---------------|-----|------|-----|
| Write command | L   | L    | ↑   |
| Write data    | L   | H    | ↑   |

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

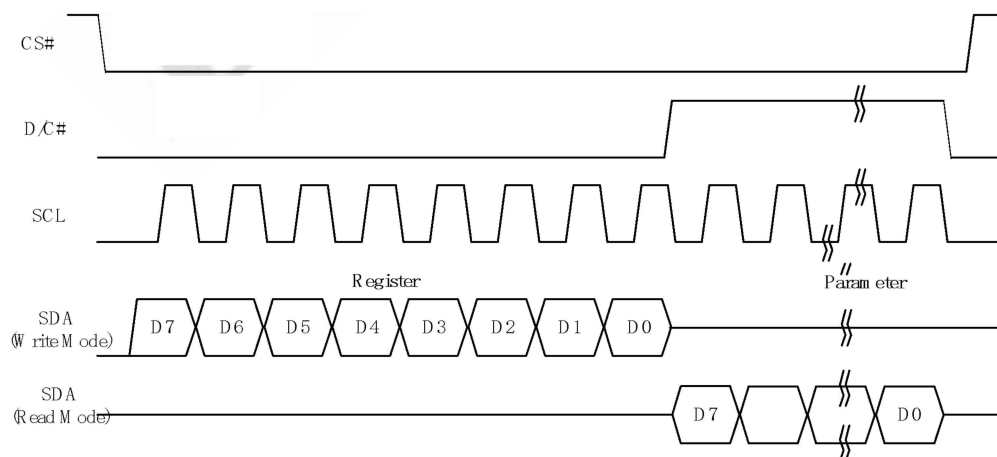
**Figure 6-1: Write procedure in 4-wire SPI mode**



In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

**Figure 6-2: Read procedure in 4-wire SPI mode**



## 6.4.3 MCU Serial Interface (3-wire SPI)

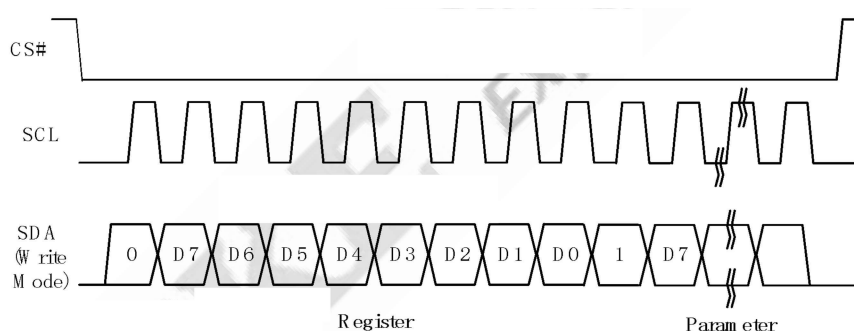
The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

| Function      | CS# | D/C# | SCL |
|---------------|-----|------|-----|
| Write command | L   | Tie  | ↑   |
| Write data    | L   | Tie  | ↑   |

Note: ↑ stands for rising edge of signal

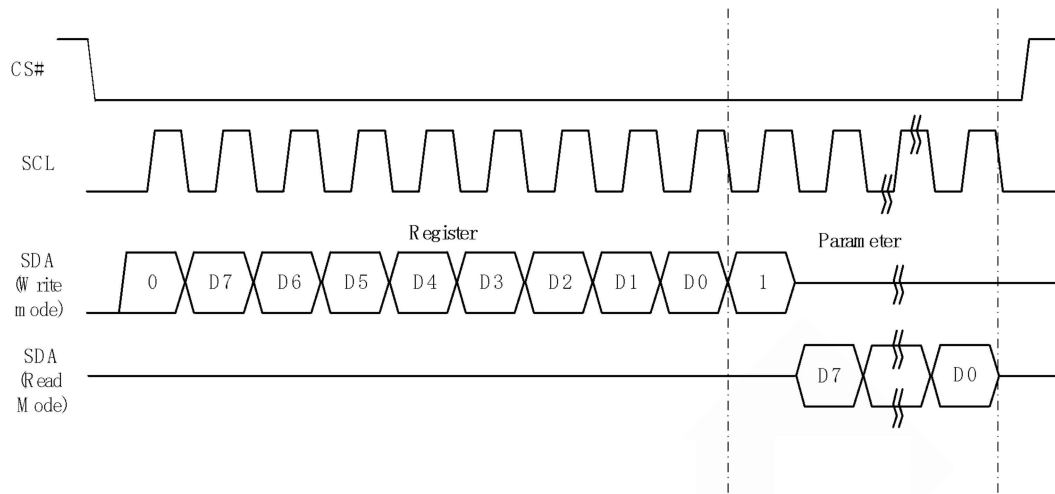
Figure 6-3: Write procedure in 3-wire SPI mode



In the Read mode:

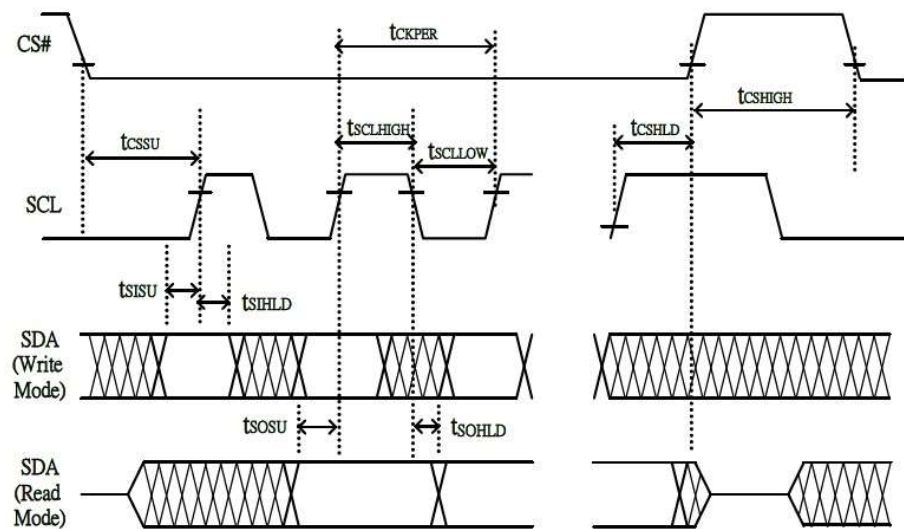
1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-4: Read procedure in 3-wire SPI mode



## 6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, T<sub>OPR</sub> =23°C.



Changed Diagram

# 深圳市英瑞达光电有限公司

## Serial Interface Timing Characteristics

(VDDIO - VSS = 2.2V to 3.7V, TOPR = 23°C, CL=20pF)

### Write mode

| Symbol   | Parameter                                                                    | Min | Typ. | Max | Unit |
|----------|------------------------------------------------------------------------------|-----|------|-----|------|
| fSCL     | SCL frequency (Write Mode)                                                   |     |      | 20  | MHz  |
| tCSSU    | Time CS# has to be low before the first rising edge of SCLK                  | 60  |      |     | ns   |
| tCSHLD   | Time CS# has to remain low after the last falling edge of SCLK               | 65  |      |     | ns   |
| tCSHIGH  | Time CS# has to remain high between two transfers                            | 100 |      |     | ns   |
| tSCLHIGH | Part of the clock period where SCL has to remain high                        | 25  |      |     | ns   |
| tSCLLOW  | Part of the clock period where SCL has to remain low                         | 25  |      |     | ns   |
| tSISU    | Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL | 10  |      |     | ns   |
| tSIHLD   | Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL   | 40  |      |     | ns   |

### Read mode

| Symbol   | Parameter                                                                | Min | Typ. | Max | Unit |
|----------|--------------------------------------------------------------------------|-----|------|-----|------|
| fSCL     | SCL frequency (Read Mode)                                                |     |      | 2.5 | MHz  |
| tCSSU    | Time CS# has to be low before the first rising edge of SCLK              | 100 |      |     | ns   |
| tCSHLD   | Time CS# has to remain low after the last falling edge of SCLK           | 50  |      |     | ns   |
| tCSHIGH  | Time CS# has to remain high between two transfers                        | 250 |      |     | ns   |
| tSCLHIGH | Part of the clock period where SCL has to remain high                    | 180 |      |     | ns   |
| tSCLLOW  | Part of the clock period where SCL has to remain low                     | 180 |      |     | ns   |
| tSOSU    | Time SO(SDA Read Mode) will be stable before the next rising edge of SCL |     | 50   |     | ns   |
| tSOHLD   | Time SO (SDA Read Mode) will remain stable after the falling edge of SCL |     | 0    |     | ns   |

# 深圳市英瑞达光电有限公司

## 7.Command Table

| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command                                 | Description                                                                                                                                                                                                                                                                                                                  |
|------|------|-----|----|----|----|----|----|----|----|----|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | 0    | 01  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | Driver Output control                   | Gate setting<br>Set A[8:0]=0127h<br>Set B[8:0]=00h                                                                                                                                                                                                                                                                           |
| 0    | 1    |     | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |                                         |                                                                                                                                                                                                                                                                                                                              |
| 0    | 1    |     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | A8 |                                         |                                                                                                                                                                                                                                                                                                                              |
| 0    | 1    |     | 0  | 0  | 0  | 0  | 0  | B2 | B1 | B0 |                                         |                                                                                                                                                                                                                                                                                                                              |
| 0    | 0    | 03  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | Gate Driving voltage control            | SetGate Driving voltage<br>A[4:0]=17h[POR], VGH at 20V[POR]<br>VGH setting from 10V to 20V                                                                                                                                                                                                                                   |
| 0    | 1    |     | 0  | 0  | 0  | A4 | A3 | A2 | A1 | A0 |                                         |                                                                                                                                                                                                                                                                                                                              |
| 0    | 0    | 04  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | Source Driving voltage control          | Set Source Driving voltage<br>A[7:0]= 41h[POR], VSH1 at 15V<br>B[7:0]=A Ch[POR], VSH2 at 5.4V<br>C[7:0]= 32h[POR], VSL at -15V                                                                                                                                                                                               |
| 0    | 1    |     | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |                                         |                                                                                                                                                                                                                                                                                                                              |
| 0    | 1    |     | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |                                         |                                                                                                                                                                                                                                                                                                                              |
| 0    | 1    |     | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |                                         |                                                                                                                                                                                                                                                                                                                              |
| 0    | 0    | 08  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | Initial Code Setting OTP Program        | Program Initial Code Setting<br>The command required CLKEN=1.<br>Refer to Register 0x22 for detail.<br>BUSY pad will output high during operation                                                                                                                                                                            |
| 0    | 0    | 09  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  | Write Register for Initial Code Setting | Write Register for Initial Code Setting Selection<br>A[7:0] ~ D[7:0]: Reserved<br>Details refer to Application Notes of Initial Code Setting                                                                                                                                                                                 |
| 0    | 1    |     | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |                                         |                                                                                                                                                                                                                                                                                                                              |
| 0    | 1    |     | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |                                         |                                                                                                                                                                                                                                                                                                                              |
| 0    | 1    |     | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |                                         |                                                                                                                                                                                                                                                                                                                              |
| 0    | 1    |     | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |                                         |                                                                                                                                                                                                                                                                                                                              |
| 0    | 0    | 0A  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | Read Register for Initial Code Setting  | Read Register for Initial Code Setting                                                                                                                                                                                                                                                                                       |
| 0    | 0    | 10  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | Deep Sleep mode                         | Deep Sleep mode Control:<br>A[1:0] : Description<br>00 Normal Mode<br>01 Enter Deep Sleep Mode 1[POR]<br>11 Enter Deep Sleep Mode 2<br>After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high.<br>Remark:<br>To Exit Deep Sleep mode, User required to send HWRESET to the driver |
| 0    | 1    |     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | A0 |                                         |                                                                                                                                                                                                                                                                                                                              |

# 深圳市英瑞达光电有限公司

|   |   |    |   |   |   |   |   |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---|---|----|---|---|---|---|---|----------------|----------------|----------------|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | 0 | 11 | 0 | 0 | 0 | 1 | 0 | 0              | 0              | 1              | Data Entry mode setting | Define data entry sequence<br>A[2:0] = 001 [POR]<br>A [1:0] = ID[1:0]<br>Address automatic increment / decrement setting<br>The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address.<br>00 - Y decrement, X decrement,<br>01 - Y decrement, X increment, [POR]<br>10 - Y increment, X decrement,<br>11 - Y increment, X increment<br>A[2] = AM<br>Set the direction in which the address counter is updated automatically after data are written to the RAM.<br>AM= 0, the address counter is updated in the X direction. [POR]<br>AM = 1, the address counter is updated in the Y direction |
| 0 | 1 |    | 0 | 0 | 0 | 0 | 0 | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

# 深圳市英瑞达光电有限公司

|   |   |    |   |    |    |    |    |    |    |    |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---|---|----|---|----|----|----|----|----|----|----|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | 0 | 0C | 0 | 0  | 0  | 0  | 1  | 1  | 0  | 0  | Booster Soft start Control | Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting.<br>A[7:0] -> Soft start setting for Phase1 = 8Bh [POR]<br>B[7:0] -> Soft start setting for Phase2 = 9Ch [POR]<br>C[7:0] -> Soft start setting for Phase3 = 96h [POR]<br>D[7:0] -> Duration setting = 0Fh [POR]<br>Bit Description of each byte:<br>A[6:0] / B[6:0] / C[6:0]:<br>Bit[6:4]<br>Driving Strength Selection<br>000 1(Weakest)<br>001 2<br>010 3<br>011 4<br>100 5<br>101 6<br>110 7<br>111 8(Strongest)<br>Bit[3:0]<br>Min Off Time Setting of GDR<br>[ Time unit ]<br>0000<br>~<br>0011<br>NA<br>0100 2.6<br>0101 3.2<br>0110 3.9<br>0111 4.6<br>1000 5.4<br>1001 6.3<br>1010 7.3<br>1011 8.4<br>1100 9.8<br>1101 11.5<br>1110 13.8<br>1111 16.5<br>D[5:0]: duration setting of phase<br>D[5:4]: duration setting of phase 3<br>D[3:2]: duration setting of phase 2<br>D[1:0]: duration setting of phase 1<br>Bit[1:0]<br>Duration of Phase<br>[Approximation]<br>00 10ms<br>01 20ms<br>10 30ms<br>11 40ms |
| 0 | 1 |    | 1 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 0 | 1 |    | 1 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 0 | 1 |    | 1 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 0 | 1 |    | 0 | 0  | D5 | D4 | D3 | D2 | D1 | D0 |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|   |   |    |   |    |    |    |    |    |    |    |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

# 深圳市英瑞达光电有限公司

|   |   |    |    |    |    |    |    |    |    |    |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                 |
|---|---|----|----|----|----|----|----|----|----|----|------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | 0 | 12 | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0  | SWRESET                                                    | It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode<br>During operation, BUSY pad will output high.<br>Note: RAM are unaffected by this command.                                                                                                                                                                                                |
| 0 | 0 | 18 | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | Temperature Sensor Control                                 | Temperature Sensor Selection<br>A[7:0] = 48h [POR], external temperature sensor<br>A[7:0] = 80h Internal temperature sensor                                                                                                                                                                                                                                                                     |
| 0 | 1 |    | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0 | 0 | 1A | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | Temperature Sensor Control (Write to temperature register) | Write to temperature register.<br>A[11:0] = 7FFh [POR]                                                                                                                                                                                                                                                                                                                                          |
| 0 | 1 |    | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0 | 1 |    | B7 | B6 | B5 | B4 | 0  | 0  | 0  | 0  |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0 | 0 | 20 | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | Master Activation                                          | Activate Display Update Sequence<br>The Display Update Sequence Option is located at R22h<br>User should not interrupt this operation to avoid corruption of panel images.                                                                                                                                                                                                                      |
| 0 | 0 | 21 | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | Display Update Control 1                                   | RAM content option for Display Update<br>A[7:0] = 00h [POR]<br>B[7:0] = 00h [POR]<br>A[7:4] Red RAM option<br>0000 Normal<br>0100 Bypass RAM content as 0<br>1000 Inverse RAM content<br>A[3:0] BW RAM option<br>0000 Normal<br>0100 Bypass RAM content as 0<br>1000 Inverse RAM content<br>B[7] Source Output Mode<br>0 Available Source from S0 to S175<br>1 Available Source from S8 to S167 |
| 0 | 1 |    | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0 | 1 |    | B7 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                 |

# 深圳市英瑞达光电有限公司

|   |   |    |   |   |   |   |   |   |   |   |                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|---|---|----|---|---|---|---|---|---|---|---|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | 0 | 22 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | Display Update Control 2 | <p>Display Update Sequence Option:<br/>           Enable the stage for Master Activation<br/>           A[7:0]= FFh (POR)<br/>           Operating sequence<br/>           Parameter<br/>           (in Hex)<br/>           Enable clock signal 80<br/>           Disable clock signal 01<br/>           Enable clock signal<br/>               Enable Analog<br/>           C0: Disable Analog<br/>               Disable clock signal<br/>           03: Enable clock signal<br/>               Load LUT with DISPLAY Mode 1<br/>               Disable clock signal<br/>           91: Enable clock signal<br/>               Load LUT with DISPLAY Mode 2<br/>               Disable clock signal<br/>           99: Enable clock signal<br/>               Load temperature value<br/>               Load LUT with DISPLAY Mode 1<br/>               Disable clock signal<br/>           B1: Enable clock signal<br/>               Load temperature value<br/>               Load LUT with DISPLAY Mode 2<br/>               Disable clock signal<br/>           B9: Enable clock signal<br/>               Enable Analog<br/>               Display with DISPLAY Mode 1<br/>               Disable Analog<br/>               Disable OSC<br/>           C7: Enable clock signal<br/>               Enable Analog<br/>               Display with DISPLAY Mode 2<br/>               Disable Analog<br/>               Disable OSC<br/>           CF: Enable clock signal<br/>               Enable Analog<br/>               Load temperature value<br/>               DISPLAY with DISPLAY Mode 1<br/>               Disable Analog<br/>               Disable OSC<br/>           F7: Enable clock signal<br/>               Enable Analog<br/>               Load temperature value<br/>               DISPLAY with DISPLAY Mode 2<br/>               Disable Analog<br/>               Disable OSC<br/>           FF: Enable clock signal<br/>               Enable Analog<br/>               Load temperature value<br/>               DISPLAY with DISPLAY Mode 1<br/>               Disable Analog<br/>               Disable OSC</p> |
|---|---|----|---|---|---|---|---|---|---|---|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

# 深圳市英瑞达光电有限公司

|   |   |    |    |    |    |    |    |    |    |    |                                      |                                                                                                                                                                                                                                                                                        |
|---|---|----|----|----|----|----|----|----|----|----|--------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | 1 |    | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |                                      |                                                                                                                                                                                                                                                                                        |
| 0 | 0 | 24 | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | Write RAM (Black White) / RAM 0x24   | After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly<br>For Write pixel:<br>Content of Write RAM(BW) = 1<br>For Black pixel:<br>Content of Write RAM(BW) = 0                                   |
| 0 | 0 | 26 | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | Write RAM (RED) / RAM 0x26)          | After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly.<br>For Red pixel:<br>Content of Write RAM(RED) = 1<br>For non-Red pixel [Black or White]:<br>Content of Write RAM(RED) = 0              |
| 0 | 0 | 2C | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 0  | Write VCOM register                  | Write VCOM register from MCU interface A[7:0] = 00h [POR]                                                                                                                                                                                                                              |
| 0 | 1 |    | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | OTP Register Read for Display Option | Read Register for Display Option:<br>A[7:0]: VCOM OTP Selection (Command 0x37, Byte A)<br>B[7:0]: VCOM Register (Command 0x2C)<br>C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes]<br>H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes] |
| 0 | 0 | 2D | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |                                      |                                                                                                                                                                                                                                                                                        |
| 1 | 1 |    | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |                                      |                                                                                                                                                                                                                                                                                        |
| 1 | 1 |    | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |                                      |                                                                                                                                                                                                                                                                                        |
| 1 | 1 |    | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |                                      |                                                                                                                                                                                                                                                                                        |
| 1 | 1 |    | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |                                      |                                                                                                                                                                                                                                                                                        |
| 1 | 1 |    | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 |                                      |                                                                                                                                                                                                                                                                                        |
| 1 | 1 |    | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 |                                      |                                                                                                                                                                                                                                                                                        |
| 1 | 1 |    | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 |                                      |                                                                                                                                                                                                                                                                                        |
| 1 | 1 |    | H7 | H6 | H5 | H4 | H3 | H2 | H1 | H0 |                                      |                                                                                                                                                                                                                                                                                        |
| 1 | 1 |    | I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 |                                      |                                                                                                                                                                                                                                                                                        |
| 1 | 1 |    | J7 | J6 | J5 | J4 | J3 | J2 | J1 | J0 |                                      |                                                                                                                                                                                                                                                                                        |
| 1 | 1 |    | K7 | K6 | K5 | K4 | K3 | K2 | K1 | K0 |                                      |                                                                                                                                                                                                                                                                                        |

# 深圳市英瑞达光电有限公司

|   |   |    |    |    |    |    |    |    |    |    |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---|---|----|----|----|----|----|----|----|----|----|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | 0 | 2F | 0  | 0  | 1  | 0  | 1  | 1  | 1  | 1  | Status Bit Read    | Read IC status Bit [POR 0x01]<br>A[5]: HV Ready Detection flag [POR=0]<br>0: Ready<br>1: Not Ready<br>A[4]: VCI Detection flag [POR=0]<br>0: Normal<br>1: VCI lower than the Detect level<br>A[3]: [POR=0]<br>A[2]: Busy flag [POR=0]<br>0: Normal<br>1: BUSY<br>A[1:0]: Chip ID [POR=01]<br>Remark:<br>A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively |
| 0 | 0 | 30 | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | Program WS OTP     | Program OTP of Waveform Setting<br>The contents should be written into RAM before sending this command.<br>The command required CLKEN=1.<br>Refer to Register 0x22 for detail.<br>BUSY pad will output high during operation                                                                                                                                                                                                    |
| 0 | 0 | 32 | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | Write LUT register | Write LUT register from MCU interface [153 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR[n] and XON[nXY]<br>Refer to Session 6.7 WAVEFORM SETTING                                                                                                                                                                                                                                               |
| 0 | 1 |    | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0 | 1 |    | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0 | 1 |    | :  | :  | :  | :  | :  | :  | :  | :  |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0 | 1 |    | :  | :  | :  | :  | :  | :  | :  | :  |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0 | 1 |    | :  | :  | :  | :  | :  | :  | :  | :  |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                 |

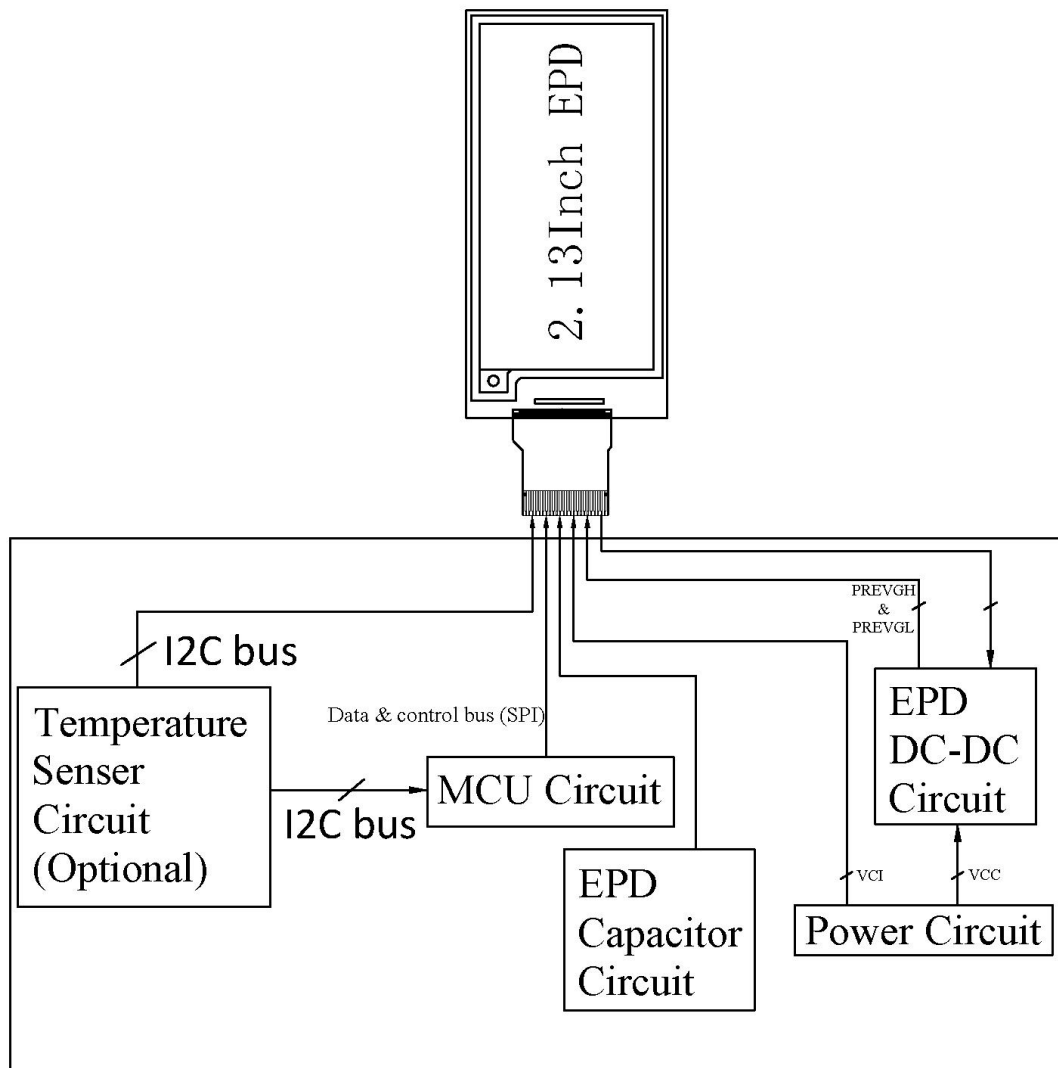
# 深圳市英瑞达光电有限公司

|   |   |    |   |   |   |   |   |   |   |   |                        |                                                                                                                                                                                                |
|---|---|----|---|---|---|---|---|---|---|---|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | 0 | 39 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | OTP<br>program<br>mode | OTP program mode<br>A[1:0] = 00: Normal Mode [POR]<br>A[1:0] = 11: Internal generated OTP<br>programming voltage<br>Remark: User is required to EXACTLY<br>follow the reference code sequences |
| 0 | 0 | 3C | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |                        | Select border waveform for VBD<br>A[7:0] = C0h [POR], set VBD as HIZ.                                                                                                                          |

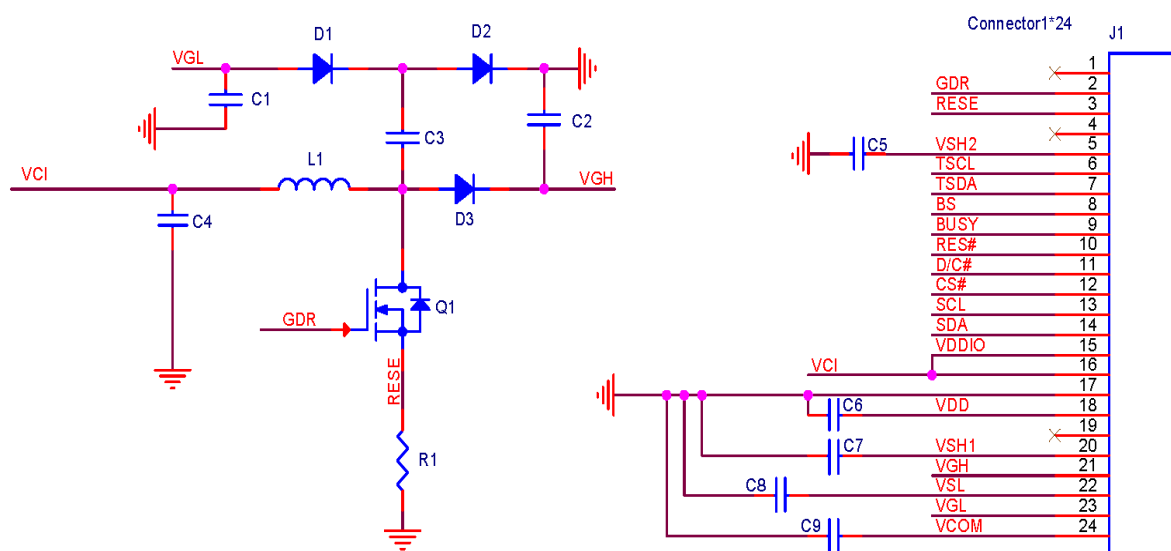
# 深圳市英瑞达光电有限公司

|   |   |    |                |                |                |                |                |                |                |                |                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|---|---|----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | 1 |    | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | 0              | 0              | A <sub>1</sub> | A <sub>0</sub> |                                          | <p>A [7:6] :Select VBD option<br/> A[7:6] Select VBD as<br/> 00 GS Transition,<br/> Defined in A[2] and<br/> A[1:0]<br/> 01 Fix Level,<br/> Defined in A[5:4]<br/> 10 VCOM<br/> 11[POR] HiZ<br/> A [5:4] Fix Level Setting for VBD<br/> A[5:4] VBD level<br/> 00 VSS<br/> 01 VSH1<br/> 10 VSL<br/> 11 VSH2<br/> A[2] GS Transition control<br/> A[2] GS Transition control<br/> 0 Follow LUT<br/> (Output VCOM @ RED)<br/> 1 Follow LUT<br/> A [1:0] GS Transition setting for VBD<br/> A[1:0] VBD Transition<br/> 00 LUT0<br/> 01 LUT1<br/> 10 LUT2<br/> 11 LUT3</p> |
| 0 | 0 | 44 | 0              | 1              | 0              | 0              | 0              | 1              | 0              | 0              | Set RAM X - address Start / End position | Specify the start/end positions of the window address in the X direction by an address unit<br>A[4:0]: XSA[4:0], X Start, POR = 01h<br>B[4:0]: XEA[4:0], X End, POR = 10h                                                                                                                                                                                                                                                                                                                                                                                             |
| 0 | 1 |    | 0              | 0              | 0              | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 0 | 1 |    | 0              | 0              | 0              | B <sub>4</sub> | B <sub>3</sub> | B <sub>2</sub> | B <sub>1</sub> | B <sub>0</sub> |                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 0 | 0 | 45 | 0              | 1              | 0              | 0              | 0              | 1              | 0              | 1              | Set Ram Y- address Start / End position  | Specify the start/end positions of the window address in the Y direction by an address unit<br>A[8:0]: YSA[8:0], Y Start, POR = 0127h<br>B[8:0]: YEA[8:0], Y End, POR = 0000h                                                                                                                                                                                                                                                                                                                                                                                         |
| 0 | 1 |    | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 0 | 1 |    | 0              | 0              | 0              | 0              | 0              | 0              | 0              | A <sub>8</sub> |                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 0 | 1 |    | B <sub>7</sub> | B <sub>6</sub> | B <sub>5</sub> | B <sub>4</sub> | B <sub>3</sub> | B <sub>2</sub> | B <sub>1</sub> | B <sub>0</sub> |                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 0 | 1 |    | 0              | 0              | 0              | 0              | 0              | 0              | 0              | B <sub>8</sub> |                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 0 | 0 | 4E | 0              | 1              | 0              | 0              | 1              | 1              | 1              | 0              | Set RAM X address counter                | Make initial settings for the RAM X address in the address counter (AC)<br>A[4:0]: XAD[4:0], POR is 01h                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 0 | 1 |    | 0              | 0              | 0              | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 0 | 0 | 4F | 0              | 1              | 0              | 0              | 1              | 1              | 1              | 1              | Set RAM Y address counter                | Make initial settings for the RAM Y address in the address counter (AC)<br>A[8:0]: YAD[8:0], POR is 0127h                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 0 | 1 |    | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 0 | 1 |    | 0              | 0              | 0              | 0              | 0              | 0              | 0              | A <sub>8</sub> |                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

## 8.Block Diagram



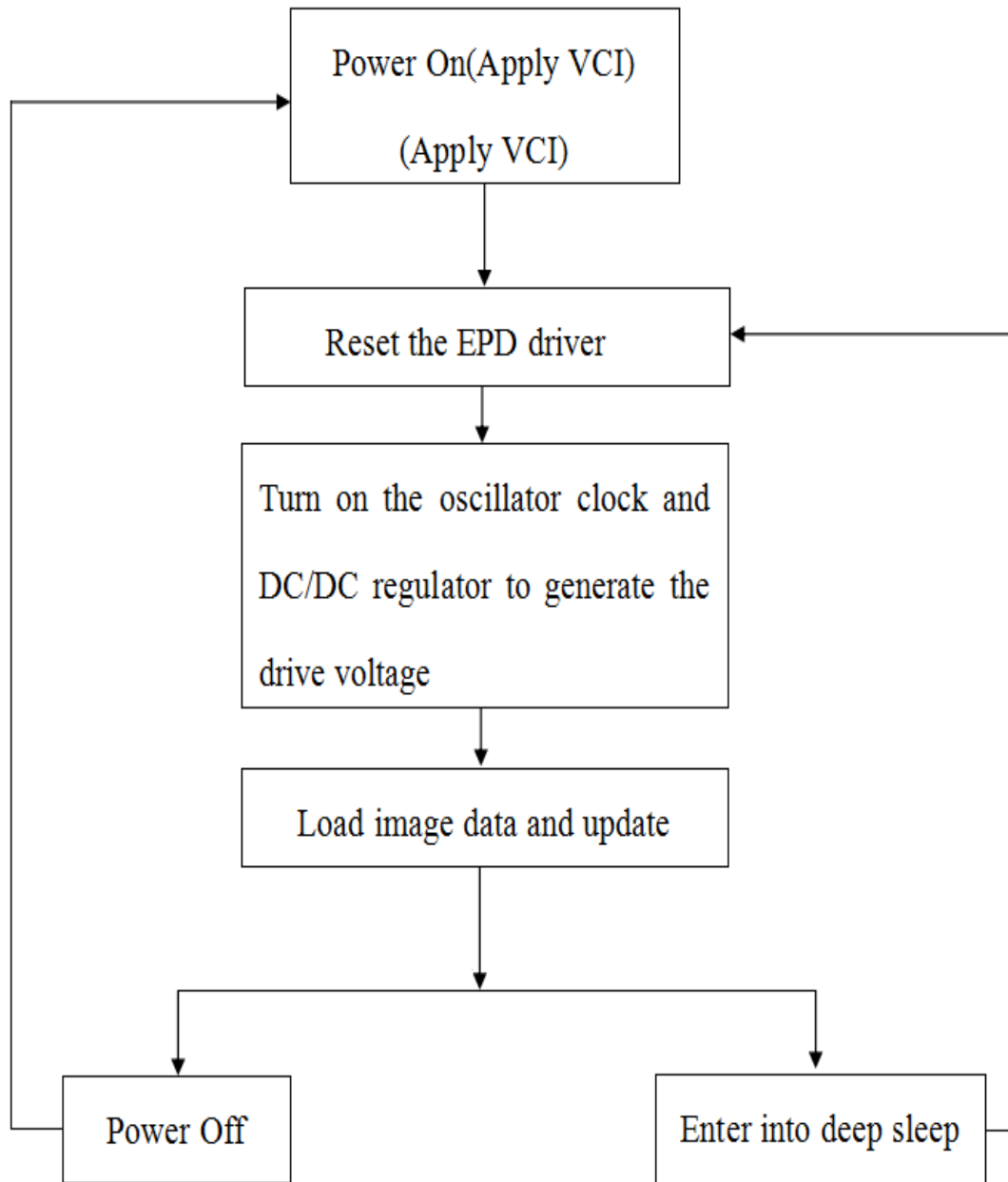
## 9. Typical Application Circuit with SPI Interface



| Part Name        | Value      | Reference Part                                                                                                                                                      |
|------------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C1C2C3<br>C5C7C8 | 1uF        | 0402/0603/0805; X5R/X7R; Voltage Rating : 25V                                                                                                                       |
| C4C6             | 1uF        | X5R/X7R; Voltage Rating : 6V or 25V                                                                                                                                 |
| C9               | 0.47uF/1uF | 0402/0603/0805; X5R/X7R; Voltage Rating : 25V                                                                                                                       |
| R1               | 2.2Ω       | 0402, 0603, 0805; 1% variation, $\geq 0.05W$                                                                                                                        |
| D1 D2 D3         | Diode      | MBR0530<br>1) Reverse DC voltage $\geq 30V$<br>2) $I_o \geq 500mA$<br>3) Forward voltage $\leq 430mV$                                                               |
| Q1               | NMOS       | Si1304BDL/NX3008NBK<br>1) Drain-Source breakdown voltage $\geq 30V$<br>2) $V_{gs(th)} = 0.9V$ (Typ), 1.3V (Max)<br>3) $R_{ds\ on} \leq 2.1\Omega$ @ $V_{gs} = 2.5V$ |
| L1               | 47uH       | CDRH2D18 / LDNP-470NC $I_o = 500mA$ (Max)                                                                                                                           |

## 10. Typical Operating Sequence

### 10.1 LUT from OTP Operation Flow



# 深圳市英瑞达光电有限公司

## 10.2 LUT from OTP Operation Reference Program Code

| ACTION                   | VALUE/DATA | COMMENT                    |
|--------------------------|------------|----------------------------|
| POWER ON                 |            |                            |
| delay                    | 10ms       |                            |
| PIN CONFIG               |            |                            |
| RESE#                    | low        | Hardware reset             |
| delay                    | 200us      |                            |
| RESE#                    | high       |                            |
| delay                    | 200us      |                            |
| Read busy pin            |            | Wait for busy low          |
| Command 0x12             |            | Software reset             |
| Read busy pin            |            | Wait for busy low          |
| SET VOLTAGE AND LOAD LUT |            |                            |
| LOAD IMAGE AND UPDATE    |            |                            |
| Command 0x24             | 4000bytes  | Load image (128/8*250)(BW) |
| Command 0x20             |            |                            |
| Read busy pin            |            | Wait for busy low          |
| Command 0x10             | Data 0X01  | Enter deep sleep mode      |
| POWER OFF                |            |                            |

# 深圳市英瑞达光电有限公司

## 11. Reliability Test

| NO | Test items                         | Test condition                                                                                                                                                             |
|----|------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1  | Low Temp.Operation                 | 0°C for 240 hrs                                                                                                                                                            |
| 2  | High Temp. High Humidity Storage   | 60°C / 80% RH for 240 hrs                                                                                                                                                  |
| 3  | Thermal Shock                      | 1cycle: -25°C / 30min ~ 60°C / 30min for 100 cycles                                                                                                                        |
| 4  | low- temperatureHumidity Storage   | 60°C/35%RH for 240hrs                                                                                                                                                      |
| 5  | High Temp. High Humidity Operation | 40°C/80%RH for 240hrs                                                                                                                                                      |
| 6  | ESD Gun                            | Air+/-4KV;Contact+/-2KV<br>Contact+/-2KV(HBMC:100pF;R:1.5k ohm)<br>Contact+/-200V(MMC:200pF;R:0 ohm)<br>(Naked EPD display,including IC and FPC area)                      |
| 7  | Vibration test                     | Frequency: 10-500Hz Direction: X, Y, Z<br>Duration: 1 hour in each direction                                                                                               |
| 8  | Dropping test                      | The test height is determined by the weight of the test object.<br>Weight ≤20KG, drop height 1000mm<br>Weight ≤50KG, drop height 500mm<br>Weight ≤100KG, drop height 250mm |

**Note:** 1. Stay white pattern for storage and non-operation test.  
2. Operation is black→white pattern, the interval is 150s.

## 12. Quality Assurance

### 12.1 Environment

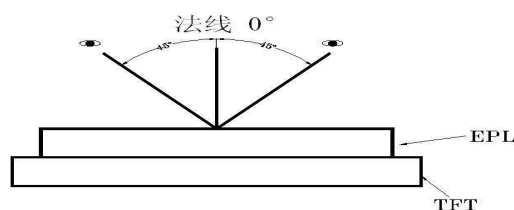
Temperature:  $23 \pm 3^{\circ}\text{C}$

Humidity:  $55 \pm 10\% \text{RH}$

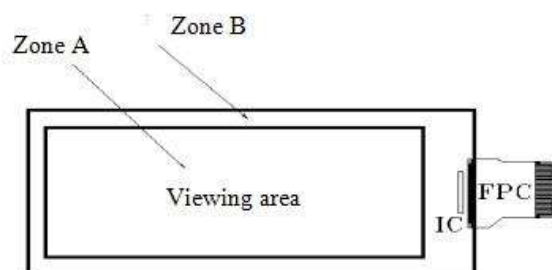
### 12.2 Illuminance

Brightness:  $1200 \sim 1500 \text{LUX}$ ; distance:  $20\text{-}30 \text{CM}$ ; Angle: Relate  $45^{\circ}$  surround.

### 12.3 Inspect method

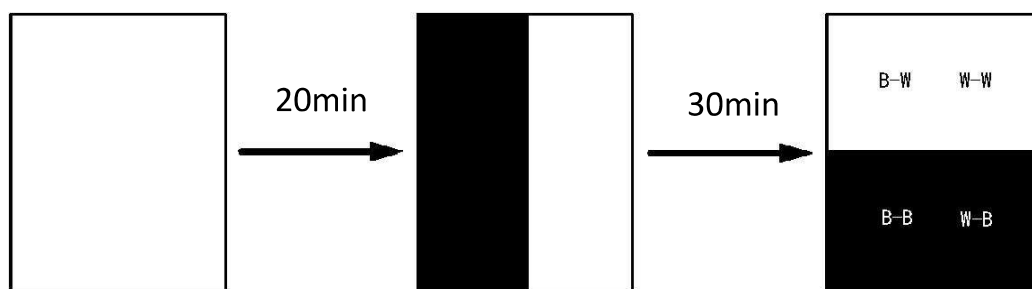


### 12.4 Display area



### 12.5 Ghosting test method

Two-color ghosting is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by Yingruida.



1) Measurement Instruments: X-rite i1Pro

2) Ghosting formula:

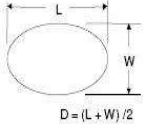
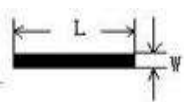
W ghosting:  $\Delta L = \text{Max} (\Delta L(\text{W-W}, \text{B-W})) - \text{Min} (\Delta L(\text{W-W}, \text{B-W}))$

K ghosting:  $\Delta L = \text{Max} (\Delta L(\text{W-B}, \text{B-B})) - \text{Min} (\Delta L(\text{W-B}, \text{B-B}))$

# 深圳市英瑞达光电有限公司

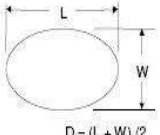
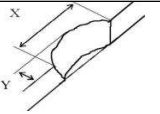
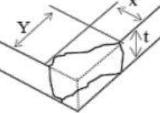
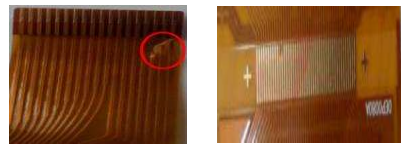
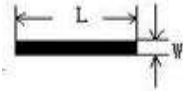
## 12.6 Inspection standard

### 12.6.1 Electric inspection standard

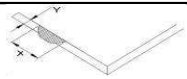
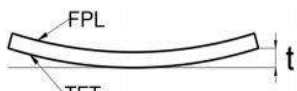
| NO. | Item                                           | Standard                                                                                                                                                                                                                                                                                                | Defect level | Method                  | Scope  |
|-----|------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------------------------|--------|
| 1   | Display                                        | Display complete<br>Display uniform                                                                                                                                                                                                                                                                     | MA           | Visual inspection       | Zone A |
| 2   | Black/White spots                              |  $D = (L + W) / 2$ $D \leq 0.25\text{mm}$ , Allowed<br>$0.25\text{mm} < D \leq 0.4\text{mm}$ 。<br>$N \leq 4$ allowable<br>$D > 0.4\text{mm}$ is not allowed                                                            | MI           | Visual Inspection card  | Zone A |
| 3   | Show B/W lines                                 |  $L \leq 0.4\text{mm}, W \leq 0.1\text{mm}$ negligible<br>$0.4\text{mm} < L \leq 1.0\text{mm}$<br>$0.1\text{mm} < W \leq 0.4\text{mm}$<br>$N \leq 4$ allowable<br>$L > 1.0\text{mm}, W > 0.4\text{mm}$ is not allowed | MI           | Visual Inspection card  | Zone A |
| 4   | Ghost image                                    | Allowed in switching process                                                                                                                                                                                                                                                                            | MI           | Visual                  | Zone A |
| 5   | Flash dot / Multilateral                       | Flash points are allowed when switching screens<br>Multilateral colors outside the frame are allowed for fixed screen time                                                                                                                                                                              | MI           | Visual/ Inspection card | Zone A |
| 6   | Segmented display                              | Selection segments are all displayed, and other segments are not displayed after the selection segment.                                                                                                                                                                                                 | MA           | Visual inspection card  | Zone A |
| 7   | Short circuit/ Circuit break/ Display abnormal | Not Allow                                                                                                                                                                                                                                                                                               | MA           | Visual                  | Zone A |
| 8   | Corner mura                                    | $X > 1\text{mm}, Y > 1\text{mm}$ , not allow<br>                                                                                                                                                                     | MI           | Visual/Ruler            | Zone A |

# 深圳市英瑞达光电有限公司

## 12.6.2 Appearance inspection standard

| NO. | Item                                              | Standard                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Defect level | Method                        | Scope      |
|-----|---------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------------------------------|------------|
| 1   | B/W spots<br>/Bubble/<br>Foreign bodies/<br>Dents |  <p> <math>D \leq 0.25\text{mm}</math> negligible<br/> <math>0.25\text{mm} &lt; D \leq 0.4\text{mm}</math> <math>N \leq 4</math> allowable<br/> <math>D &gt; 0.4\text{mm}</math> is not allowed         </p>                                                                                                                                                                                                                                                                                                                                                                                                     | MI           | Visual/<br>inspection<br>Card | Zone A     |
| 2   | Chips/Scratch/<br>Edge crown                      |  <p> <math>X \leq 3\text{mm}, Y \leq 0.5\text{mm}</math> <math>t =</math> not counted, and without affecting the electrode, permissible         </p>  <p> <math>2\text{mm} \leq X</math> or <math>2\text{mm} \leq Y</math> <math>t =</math> not counted, and without affecting the electrode, permissible         </p>  <p> <math>W \leq 0.1\text{mm}, L \leq 5\text{mm}</math>, without affecting the electrode, <math>n \leq 2</math> </p> | MI           | Visual / Ruler                | Zone A/B   |
| 3   | TFT Cracks                                        |  <p>Not Allow</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | MA           | Visual<br>/ Microscope        | Zone A/B   |
| 4   | Dirty/<br>foreign body                            | Allowed if can be removed                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | MI           | Visual /<br>clean cloth       | Zone A / B |
| 5   | FPC broken/<br>Goldfingers<br>oxidation/ scratch  |  <p>Not Allow</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | MA           | Visual<br>/ Microscope        | Zone B     |
| 6   | B/W Line                                          |  <p> <math>L \leq 0.4\text{mm}, W \leq 0.1\text{mm}</math> negligible<br/> <math>0.4\text{mm} &lt; L \leq 1.0\text{mm}</math><br/> <math>0.1\text{mm} &lt; W \leq 0.4\text{mm}</math><br/> <math>N \leq 4</math> allowable<br/> <math>L &gt; 1.0\text{mm}, W &gt; 0.4\text{mm}</math> is not allowed         </p>                                                                                                                                                                                                                                                                                              | MI           | Visual / Ruler                | Zone A     |

# 深圳市英瑞达光电有限公司

|    |                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |    |                            |          |
|----|--------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----------------------------|----------|
| 7  | TFT edge bulge<br>/TFT chromatic aberration      |  <p>TFT edge bulge:<br/> <math>X \leq 3\text{mm}</math>, <math>Y \leq 0.3\text{mm}</math> Allowed<br/>           TFT chromatic aberration :Allowed</p>                                                                                                                                                                                                                                                             | MI | Visual<br>/ Microscope     | Zone A/B |
| 8  | Electrostatic point                              | <p><math>D \leq 0.2\text{mm}</math>, allow<br/> <math>0.2\text{mm} &lt; D \leq 0.35\text{mm}</math>, <math>n \leq 4</math> allow<br/> <math>D &gt; 0.35\text{mm}</math> is not allowed<br/>           (<math>n \leq 5</math> items are allowed within 5 mm in diameter)</p>                                                                                                                                                                                                                         | MI | Visual<br>/inspection card | Zone A   |
| 9  | PCB damaged/<br>Poor welding/<br>Curl            | <p>PCB (Circuit area) damaged Not Allow<br/>           PCB Poor welding Not Allow<br/>           PCB Curl <math>\leq 1\%</math></p>                                                                                                                                                                                                                                                                                                                                                                 | MA | Visual / Ruler             | Zone B   |
| 10 | Edge glue height/<br>Edge glue bubble            | <p>Edge Adhesives <math>H \leq</math> PS surface<br/>           (Including protect film)<br/>           Edge adhesives overflow onto protect film <math>\leq 1/2</math> FPL to PS Margin width<br/>           Length excluding<br/>           Edge adhesives seep in <math>\leq 1/2</math> FPL<br/>           Margin width Length excluding<br/>           Edge adhesives bubble: bubble Width <math>\leq 1/2</math> Margin width; Length <math>\leq 5.0\text{mm}</math>. <math>n \leq 5</math></p> | MI | Visual / Ruler             | Zone B   |
| 11 | Protect film                                     | Surface scratch but not effect protect function, Allowed                                                                                                                                                                                                                                                                                                                                                                                                                                            | MI | Visual                     | Zone A/B |
| 12 | Silicon glue                                     | <p>Thickness <math>\leq</math> PS surface (With protect film); Full cover the IC;<br/>           Shape:<br/>           The width on the FPC <math>\leq 1.0\text{mm}</math> (Front)<br/>           The width on the FPC <math>\leq 1.0\text{mm}</math> (Back)<br/>           smooth surface, No obvious raised.</p>                                                                                                                                                                                  | MI | Visual/Ruler               | Zone B   |
| 13 | Warp degree (TFT substrate)                      |  <p><math>t \leq 1.0\text{mm}</math></p>                                                                                                                                                                                                                                                                                                                                                                         | MI | Ruler                      | Zone B   |
| 14 | Color difference in COM area (Silver point area) | Allowed                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | MI | Visual                     | Zone B   |
| 15 | Corner and edge damage of FPL                    | <p>Corner and edge damage <math>\leq 1/2</math> border width</p>                                                                                                                                                                                                                                                                                                                                                 | MI | Visual / Ruler             | Zone A   |

## 13.Packaging

### PACKING INSTRUCTION

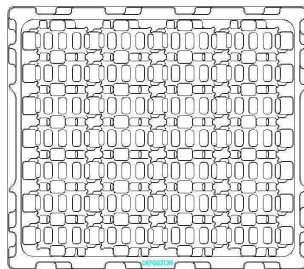
| P/N     | Customer Code | Ref. P/N | Type  | PKG Method | Marking | Surface Marks | Pull Tape |
|---------|---------------|----------|-------|------------|---------|---------------|-----------|
| YRD0213 |               |          | GLASS | Blister    | BACK    | None          | YES       |

| Packing Materials List |                          |           |      |       | 28PCS/LAYER, 20LAYER/CTN, TOTAL 560PCS/CTN.                                                     |
|------------------------|--------------------------|-----------|------|-------|-------------------------------------------------------------------------------------------------|
| List                   | Model                    | Materials | Q'ty | Unit  | Pull tape:<br> |
| Carton                 | 7# 417*362*229 mm        | corrugate | 1    | Piece |                                                                                                 |
| Inner Carton           | 7#(INNER) 400*343 *95 mm | corrugate | 2    | Piece |                                                                                                 |
| Blister                | YRD0213N                 | PET       | 22   | Piece |                                                                                                 |
| Thin foam              | 291.30*265.80*11.5-1.8mm | EPE       | 20   | Piece |                                                                                                 |
| Antistatic vacuum bag  | 450*590*0.075            |           | 2    | Piece |                                                                                                 |
| Foam board             | Yingruida2251-10         | EPE       | 3    | Piece |                                                                                                 |
| PULL TAPE              | 16*5*10.05               |           | 560  | Piece |                                                                                                 |

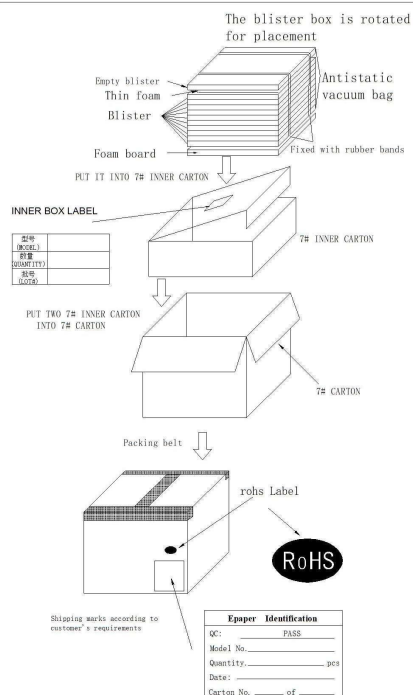
Detail:

Blister box:

Note: there are 20 layers of products, divided into 2 inner boxes, and an empty blister box is placed on the top of each inner box, so the number of blister boxes is 22



QUANTITY: 28PCS



# 深圳市英瑞达光电有限公司

## 14. Handling, Safety, and Environment Requirements

### Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

### Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

| Data sheet status                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                        |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------|
| Product specification                                                                                                                                                                                                                                                                                                                                                                                                                                     | This data sheet contains final product specifications. |
| Limiting values                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                        |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |                                                        |
| Application information                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                                        |
| Where application information is given, it is advisory and does not form part of the specification.                                                                                                                                                                                                                                                                                                                                                       |                                                        |
| Product Environmental certification                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                        |
| ROHS                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                        |
| REMARK                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                        |
| All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.                                                                                                                                                                       |                                                        |
| Transport environment                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                        |
| When the humidity of transportation environment is between 45%RH~70%RH, the product can be stored for 30 days, and the product can be stored for 10 days if it is lower or higher than this range                                                                                                                                                                                                                                                         |                                                        |